IDC PA

QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	09/663663	Prepared by	QI	Tracking Number	58877461
Examiner-GAU	Coleman 2823	Date	3-11-04	Week Date	1-12-04
		No. of queries	1	IEW	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE In the renumbering of claims, claim 3 now depends on claim 4 (original claim 2) and claim 7 depends on claim 8 (original claim 12).

Please correct dependency

Thank you

initials QI

RESPONSE Corrected (i.e. renumbered claims)

initials

E-5 (Rev. 10/01/02)

Issue Classification	Application No.	Applicant(s)	
	09/665,663	UEDA, SHIGEYUKI	
	Examiner	Art Unit	
	W. David Coleman	2823	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
257	777		

INTERNATIONAL CLASSIFICATION	
H01L	23/28
H01L	23/52
H01L	29/40
	/
	/

None
(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date) 1/1/04

W. DAVID COLEMAN
PRIMARY EXAMINER

(Primary Examiner) (Date) 1/1/04

Total Claims Allowed: 10

O.G. Print Claim(s)	O.G. Print Fig.
1	2

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
2	2		32		62		92		122		152		182
3	3		33		63		93		123		153		183
4	4		34		64		94		124		154		184
5	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
7	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
8	10		40		70		100		130		160		190
1	11		41		71		101		131		161		191
6	12		42		72		102		132		162		192
9	13		43		73		103		133		163		193
10	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Issue Classification	Application No.	Applicant(s)	
	09/665,663	UEDA, SHIGEYUKI	
	Examiner	Art Unit	
	W. David Coleman	2823	

ISSUE CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)
257	777		
INTERNATIONAL CLASSIFICATION			
H01L	23/28		
H01L	23/52		
H01L	29/40		
	/		
	/		

None
(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

W. David Coleman
Primary Examiner
(Primary Examiner) (Date) 12/13/03

Total Claims Allowed: 10

O.G. Print Claim(s)	O.G. Print Fig.
1	2

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
2	2		32		62		92		122		152		182
3	3		33		63		93		123		153		183
4	4		34		64		94		124		154		184
5	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
7	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
8	8		40		70		100		130		160		190
1	1		41		71		101		131		161		191
6	6		42		72		102		132		162		192
9	9		43		73		103		133		163		193
10	10		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

CLMPTO 12/16/03

CLAIM 1 (CANCELLED)

2 (Amended) The semiconductor chip according to claim 11, wherein said semiconductor chip is overlapped with and joined to a surface of another solid device in a state where said surface protective film is opposed to a surface of the solid device.

3 (Amended) The semiconductor chip according to claim 2, further comprising

an internal connection pad which is formed by partially exposing said the internal wiring from said surface protective film in a portion of different from said external connection pad, and

an electrical contact projection formed in a raised state on the internal connection pad using a metal material having oxidation resistance in order to make electrical connection to the said solid device.

4. The semiconductor chip according to claim 2, wherein

said solid device includes another semiconductor chip.

5 (Amended) The semiconductor chip according to claim 3, wherein

said wire connecting portion is composed of the same material as that for said electrical contact projection.

CLAIM 6 (CANCELLED)

7. (Twice Amended) The semiconductor chip according to claim 12, wherein

said wire connecting portion is composed of the same material as that for said electrical contact projection.

CLAIM 8-9 (CANCELLED)

10. (Amended) The semiconductor chip according to claim 12, further comprising a lead frame and a bonding wire, the bonding wire electrically interconnecting the lead frame and the wire connecting portion.

11. (Amended) A semiconductor chip adapted for electrical connection to an external terminal, comprising:

a semiconductor chip body having a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad, both the external connection pad and the internal connection pad facing in a same direction as the surface of the semiconductor chip body;

a wire connecting portion fabricated from a metal material having oxidation resistance and electrically connected to the external connection pad;

an electrical contact projection fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad;

a surface protective film covering the internal wiring and the surface of the semiconductor chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film; and

a wire electrically connected to the segment of the wire connecting portion for connecting the semiconductor chip to the external terminal, wherein

the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

6 12. (Amended) A semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a primary chip, wherein

said primary chip comprises

a primary chip body having a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad, both the external connection pad and the internal connection pad facing in a same direction as the surface of the primary chip body;

a wire connecting portion fabricated from a metal material having oxidation resistance and electrically connected to the external connection pad;

an electrical contact projection fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad, the electrical contact projection operative to electrically connect the primary and secondary chips together; and

a surface protective film covering the internal wiring and the surface of the primary chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film, wherein

the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

9 -- 13. (NEW) The semiconductor chip according to claim 11, wherein the wire connection portion and the electrical contact projection are made of the same material and have simultaneously been formed.

10 14. (NEW) The semiconductor chip according to claim 12, wherein the wire connection portion and the electrical contact projection are made of the same material and have simultaneously been formed. --